Imperial College London

Problem Class 5

Timing Constraints (Problem Sheet 4)

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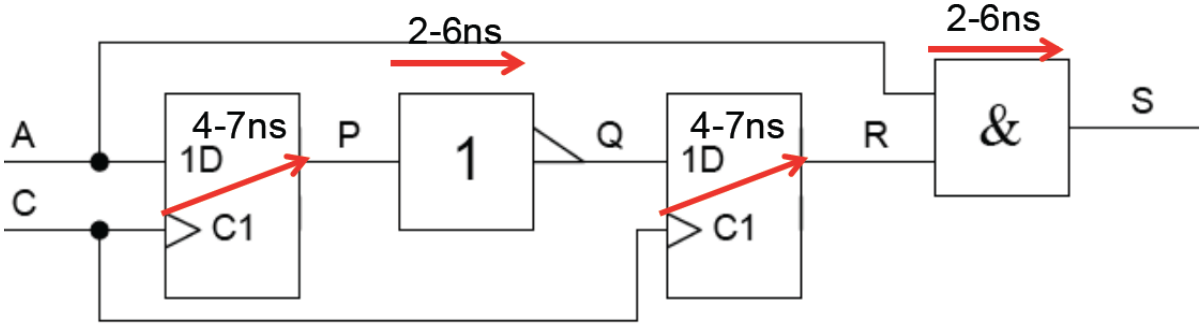
Problem 1: Test yourself (not in tutorial sheet)

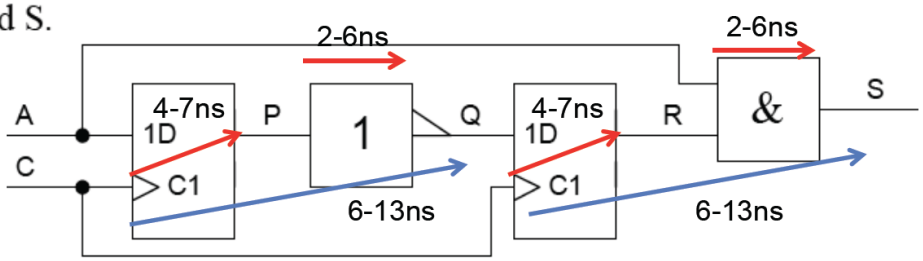
In the circuit below the propagation delay of the flipflops may vary between 4 and 7 ns while the propagation delay of the gates may vary between 2 and 6 ns.

Calculate the minimum and the maximum propagation delays from each of A and C to each of P, Q and R and S.



Solution 1: Test yourself

Calculate the minimum and the maximum propagation delays from each of A and C to each of P, Q and R and S.



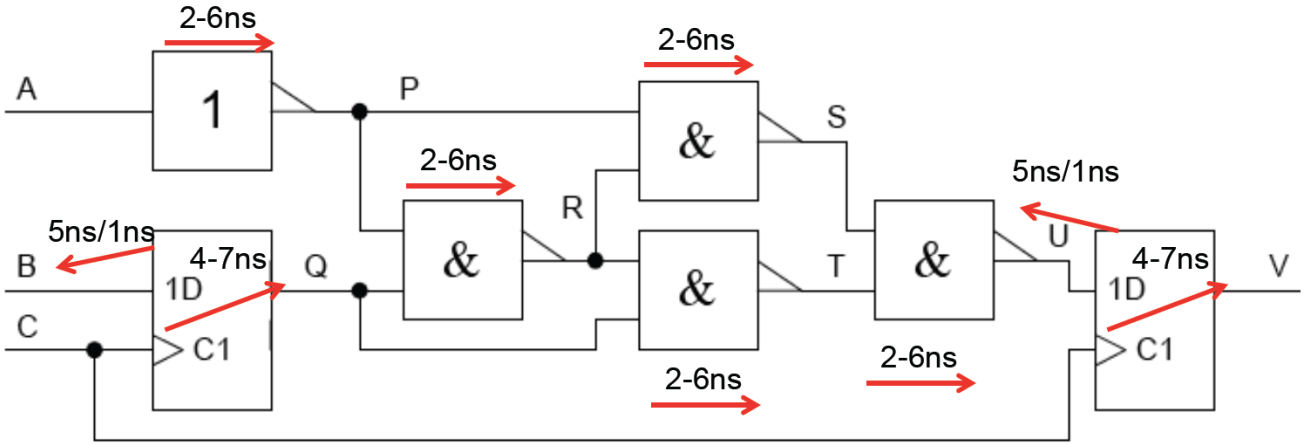
This is a trick question: there is no propagation delay between A and any of P, Q or R since a transition in A does not directly cause any of these other signals to change. The min and max delays from A to S are 2 and 6 ns. Of course if R happens to be low, there is no propagation delay between A and S either.

The min and max delays from C to P, Q, R and S are 4 and 7, 6 and 13, 4 and 7, and 6 and 13 ns respectively. The important point to realise is that since a transition at Q does not directly cause R to change, it follows that there is no delay path through both flipflops. The expression for a propagation delay **never** involves more than one flipflop delay.

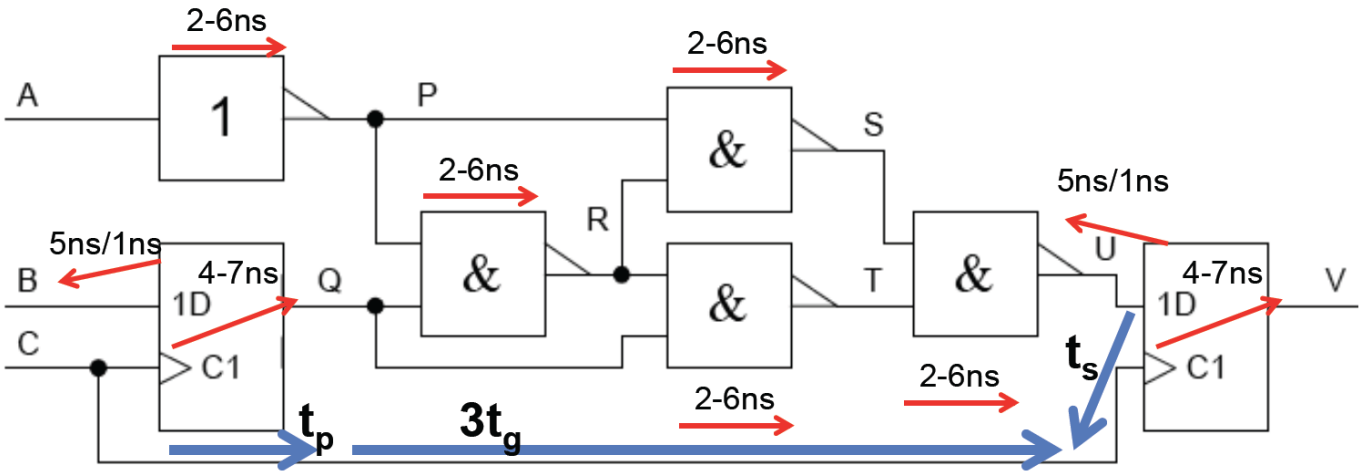
Problem 2: Explain it (Not in tutorial sheet)

In the circuit below the setup and hold times of the flipflops are 5 ns and 1 ns respectively. The propagation delay of the flipflops may vary between 4 and 7 ns while the propagation delay of the gates may vary between 2 and 6 ns.

Calculate the minimum and the maximum propagation delays between C and U. Hence calculate the maximum frequency of the clock, C.



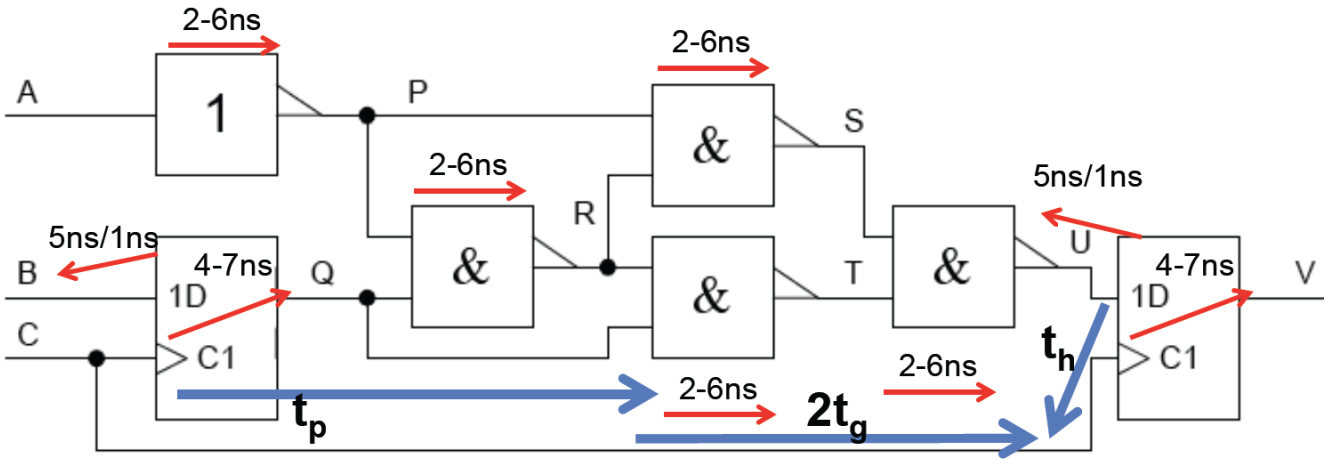
Solution 2: Explain it – Setup requirement



The longest path from C to U passes through the flipflop and then through three gates: this gives a maximum propagation delay of 25 ns. This happens when A=0⇒P=1⇒R=!Q⇒T=1⇒U=!S=R=!Q. We therefore use $3t_g$ in the setup inequality below.

Setup: $t_p + 3t_g + t_s < T \Rightarrow T > 7 + 3\times 6 + 5 = 30\ \text{ns} \Rightarrow f < 33\ \text{MHz}$

Solution 2: Explain it – hold requirement



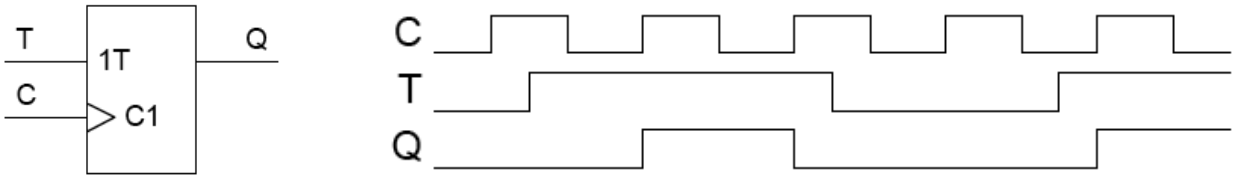
The shortest path from C to U passes through the flipflop and then through two gates: this gives a minimum propagation delay of 8 ns. This happens when A=1⇒P=0⇒R=S=1⇒U=!T=Q. We therefore use $2t_g$ in the hold inequality below.

Hold: $t_h < t_p + 2t_g \quad \Rightarrow \quad 1 < 4 + 2\times 2 = 8$ ✓

Problem 3: Test yourself (Sheet 4 Q1)

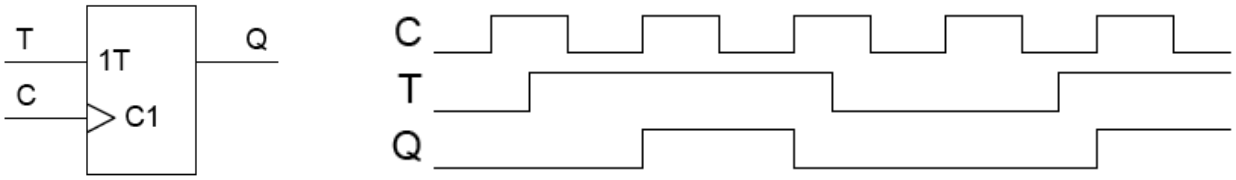
A toggle flipflop (T-flipflop) changes state whenever its T input is high on the CLOCK ↑ edge as shown in the timing diagram.

Show how a T-flipflop can be made by combining an XOR gate with a D-flipflop.

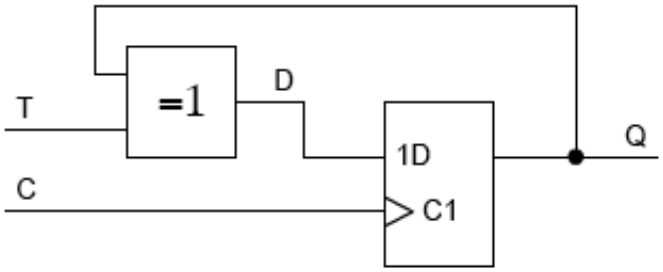


Solution 3: Test yourself (Sheet 4 Q1)

Show how a T-flipflop can be made by combining an XOR gate with a D-flipflop.

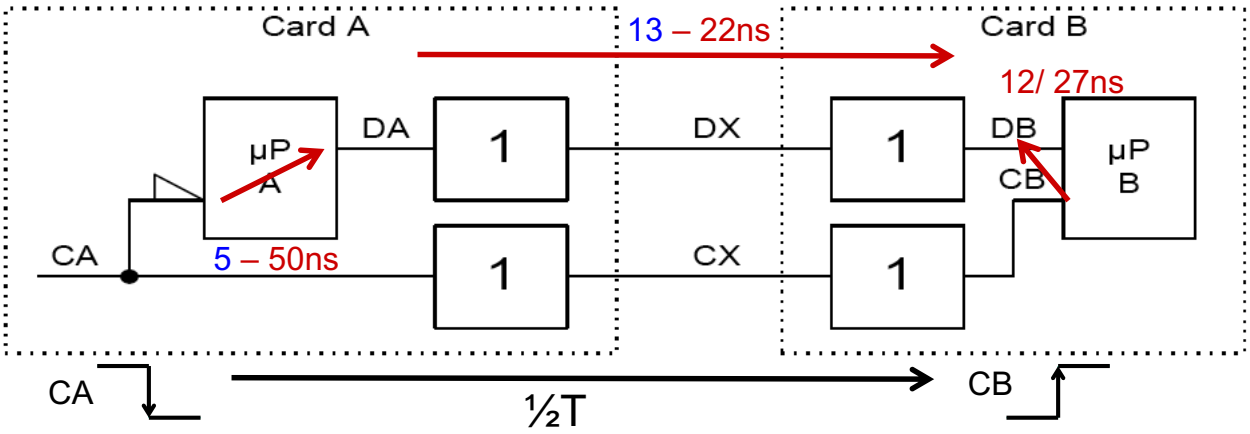


An XOR gate can be used to invert a signal or pass it through unchanged according to whether a control input is high or low.

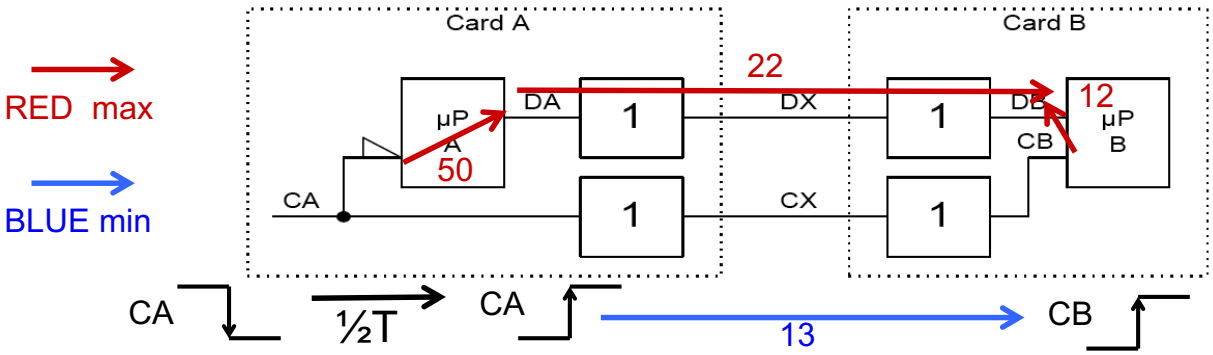


Problem 4: Explain it (Sheet 4 Q2)

A multi-processor system contains two microprocessors which are mounted on separate printed circuit cards. The clock and data signals pass through a line driver when they leave one card and a line receiver when they pass onto the next. The combined delay of the driver+receiver may vary between 13 ns and 22 ns. New data values appear at DA on the falling edge of CA with a propagation delay of 5 to 50 ns. Data is clocked into µP B on the rising edge of CB with a setup time of 12 ns and a hold time of 27 ns. If the clock, CA, is a symmetrical squarewave, calculate its maximum frequency.



Solution 4: Explain it (Sheet 4 Q2)



We define t=0 as the falling edge of CA.

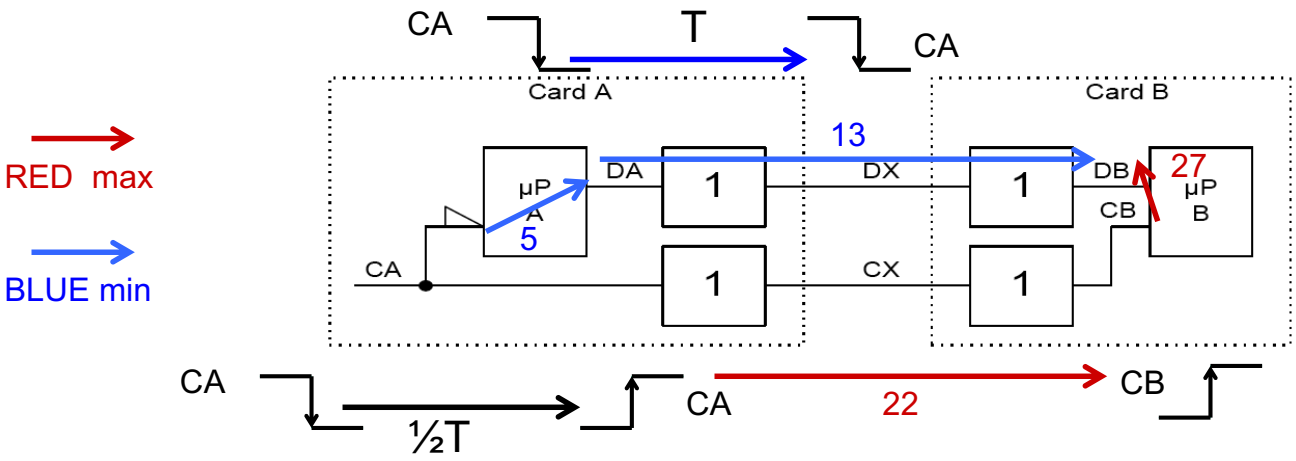
Setup requirement: $\max(DB\uparrow\downarrow)+12 < \min(CB\uparrow)$

$50+22+12 < (13 + ½T)$

$½T > 71 \Rightarrow f < 7$ MHz

Setup time requirement is governed by the **slowest data signal path relative to fastest clock path**

Solution 4: Explain it (Sheet 4 Q2)



Hold requirement: $\max(CB\uparrow) + 27 > \min(T + DB\uparrow\downarrow)$

$\frac{1}{2}T + 22 + 27 > T + 5 + 13$

$\frac{1}{2}T > 31$ (less severe restriction than above)

Hold time requirement is governed by the **fastest data signal path on successive cycles relative to slowest clock path**